INCREASED EFFICIENCY IN QAM POWER AMPLIFIERS

D.R. Conn and R.H. Hemmers

Department of Electrical and Computer Engineering, McMaster University
Hamilton, Ontario, Canada L8S 4L7

ABSTRACT

A dynamic biasing procedure designed to improve the average dc-rf conversion efficiency of power amplifiers employing multi-level modulation schemes such as QAM is investigated. In this technique, the gate bias voltage is adjusted in accordance with the phasor currently being transmitted. Simulations show promising results for a 1W class-A mode power amplifier. A system to address the distortion issue and dynamic bias control is proposed.

INTRODUCTION

The use of non-constant envelope bandwidth-efficient signalling schemes such as quadrature amplitude modulation (QAM) will cause a severe drop in average dc-rf efficiency of linear power amplifiers. Hence, it is necessary and timely to investigate techniques to achieve increased efficiency under the constraint of low distortion for use in multi-carrier CDMA/TDMA/GSM systems.

A technique proposed in the literature [1-4] involves dynamically changing the bias voltage in proportion to the signal envelope. This approach improves the overall efficiency of class-A mode power amplifiers. The prime motivation behind adaptively modifying the bias voltage with reduced rf drive level lies in the reduction of dc supply power resulting in increased dynamic dc-rf efficiency. This occurs while still maintaining the appropriate levels of voltage and current excursions to achieve the required output power from the amplifier. Unfortunately, variations in bias voltage cause gain and phase distortion in the output signal which need to be addressed.

The dynamic gate bias technique is analysed with reference to a class-A amplifier using QAM. Although reference is made to 16-QAM throughout, the concept is easily generalized to *M*-QAM. As a practical example, we demonstrate the approach using a realistic FET model and harmonic-balance analysis employing the CAD system OSA90/hope™ [5]. Then a practical system is proposed to implement the technique addressing nonlinear distortion and bias control.

CONSTANT GATE BIAS

Consider the constellation shown in Fig. 1. In general, this type of multi-level modulation scheme groups N bits into one signalling symbol yielding 2^N constellation points or phasors, each having different amplitude and phase values. For the 16-QAM case, the normalized output signal amplitudes $\hat{V}_{\text{out}}^{(i)}$ are given by the multipliers $\sqrt{2}$, $\sqrt{10}$ and $3\sqrt{2}$ corresponding to the points (1,1), (1,3) and (3,3) in the constellation diagram of Fig 1.

We can expect the dc-rf efficiency of a power amplifier to be adversely affected by the application of such multi-level modulated signals. To demonstrate the severity of the problem, consider an ideal class-A power amplifier with a classic 50% maximum dc-rf efficiency $\eta_{\text{dc}}^{\max}$ where we define

$$\eta_{\text{dc}} \equiv \frac{P_{\text{out}}}{P_{\text{dc}}} \tag{1}$$

with P_{out} representing the fundamental rf output power and P_{dc} as the dc supply power. Assuming that $\eta_{\text{dc}}^{\max}$ corresponds to the high-level phasors, i.e., $V_{\text{out}}^{(3)} = k\hat{V}_{\text{out}}^{(3)} = k3\sqrt{2}$, with k as a proportionality constant, the power delivered to an optimal load R_{L} is

$$P_{\text{out}}^{(3)} = \frac{|V_{\text{out}}^{(3)}|^2}{2R_{\text{L}}} = \frac{|k3\sqrt{2}|^2}{2R_{\text{L}}} = \frac{9k^2}{R_{\text{L}}} \tag{2}$$

and since $\eta_{\text{dc}}^{(3)} = 0.5$,

$$P_{\text{dc}} = 2P_{\text{out}}^{(3)} = \frac{18k^2}{R_{\text{L}}} \tag{3}$$

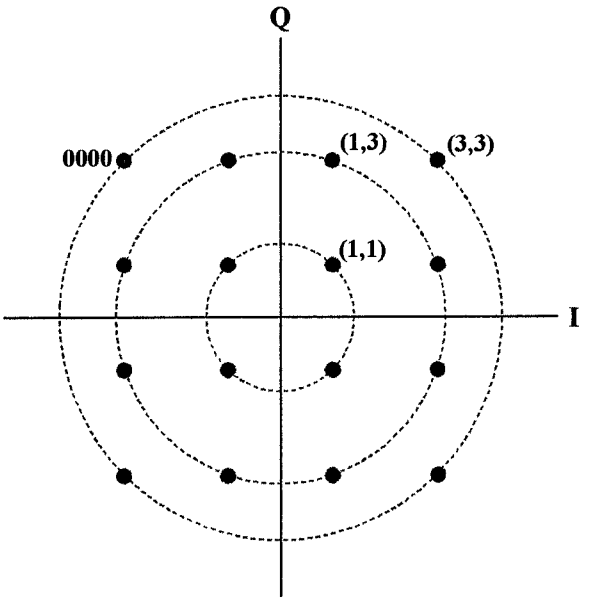

Fig. 1. Square 16-QAM constellation illustrating three distinct signal amplitude levels.

For a conventional fixed gate bias, assume P_{dc} remains constant, then for the mid-level phasors

$$P_{out}^{(2)} = \frac{|k\hat{V}_{out}^{(2)}|^2}{2R_L} = \frac{|k\sqrt{10}|^2}{2R_L} = \frac{5k^2}{R_L} \quad (4)$$

which yields a dc-rf efficiency of

$$\eta_{dc}^{(2)} = \frac{P_{out}^{(2)}}{P_{dc}} \approx 0.278 \quad (5)$$

For the low-level phasors,

$$P_{out}^{(1)} = \frac{|k\hat{V}_{out}^{(1)}|^2}{2R_L} = \frac{|k\sqrt{2}|^2}{2R_L} = \frac{k^2}{R_L} \quad (6)$$

which yields

$$\eta_{dc}^{(1)} = \frac{P_{out}^{(1)}}{P_{dc}} \approx 0.056 \quad (7)$$

Thus, for a square 16-QAM signalling scheme with the above assumptions and with all constellation points having equal probability of occurrence, the average dc-rf efficiency is

$$\eta_{dc}^{avg} = \frac{1}{2^N}\left[\sum_{i=1}^{3} a_i \eta_{dc}^{(i)}\right] = \frac{1}{2^N}\left[4\eta_{dc}^{(1)} + 8\eta_{dc}^{(2)} + 4\eta_{dc}^{(3)}\right] \quad (8)$$

or 27.8 %. Fig. 2 illustrates these results graphically for the case of a constant gate bias voltage applied to an ideal class-A amplifier with constant dc supply power. We can clearly see how dramatically the dc-rf efficiency drops for the lower-level phasors.

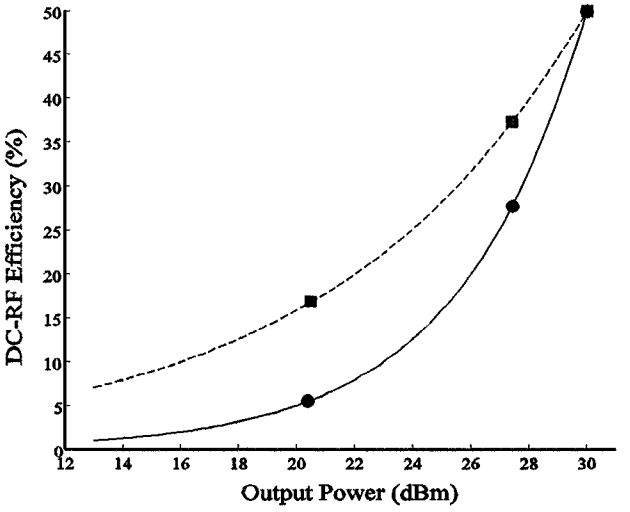

Fig. 2. DC-RF efficiency vs. output power for an ideal 1W class-A mode amplifier using fixed (——) and dynamic (– – –) gate bias; (●) and (■) correspond to the three distinct signal amplitudes for 16-QAM.

DYNAMIC GATE BIAS

One simple technique to improve the average dc-rf efficiency involves adjusting the gate bias voltage in accordance with the phasor currently being transmitted. Fig. 3 shows qualitatively a simplified FET I-V characteristic. The load resistance R_L for optimal efficiency determines the maximum excursion of drain current and voltage. For class-A mode operation, the operating point Q_3 yields a dc-rf efficiency of 50% corresponding to the high-level 16-QAM phasors. The geometry of the load line gives

$$\frac{I_{dd}}{V_{dd}} = \frac{1}{R_L} = \frac{\alpha I_{dd}}{V_p^{(2)}} = \frac{\beta I_{dd}}{V_p^{(1)}} \quad (9)$$

where $V_p^{(2)} = \alpha V_{dd}$ and $V_p^{(1)} = \beta V_{dd}$. Using the expression $P_{out} = V_p^2 / 2R_L$, including $R_L = V_{dd} / I_{dd}$, $P_{dc}^{(2)} = V_{dd}(\alpha I_{dd})$ and $P_{dc}^{(1)} = V_{dd}(\beta I_{dd})$, we obtain

$$\eta_{dc}^{(Q_2)} = \frac{\alpha}{2} \quad \text{and} \quad \eta_{dc}^{(Q_1)} = \frac{\beta}{2} \quad (10)$$

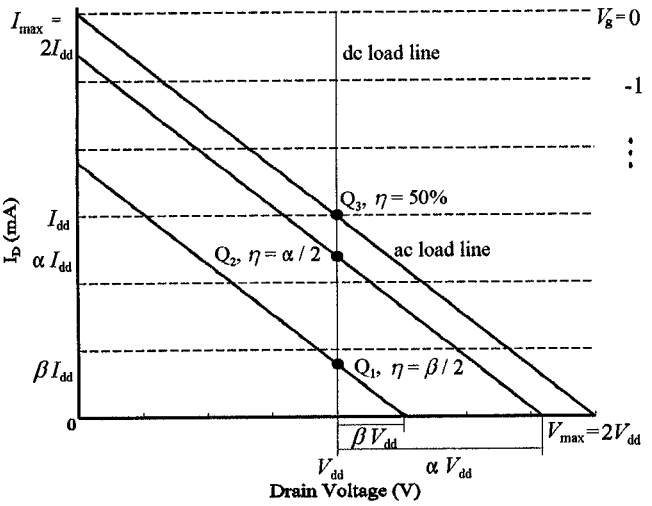

Fig. 3. Simplified FET I-V characteristic showing the ac load lines for different gate bias operating points. Bias at Q_3 for high-level 16-QAM phasors to obtain 50% efficiency. Bias at Q_2 and Q_1 for mid- and low-level phasors.

Therefore, for the high-level phasors ($\eta_{dc}^{(3)} = 0.5$) $V_{out}^{(3)} = V_{dd} = k3\sqrt{2}$ which is solved to yield $k = V_{dd}/3\sqrt{2}$. Hence, using the expressions $V_{out}^{(2)} = \alpha V_{dd} = k\sqrt{10}$ and (10) we obtain

$$\alpha = \frac{\sqrt{10}}{3\sqrt{2}} \quad \Rightarrow \quad \eta_{dc}^{(2)} = \frac{\sqrt{5}}{6} \approx 0.373 \qquad (11)$$

Similarly, for the low-level phasors $V_{out}^{(1)} = \beta V_{dd} = k\sqrt{2}$ hence,

$$\beta = \frac{1}{3} \quad \Rightarrow \quad \eta_{dc}^{(1)} = \frac{1}{6} \approx 0.167 \qquad (12)$$

Therefore, by applying the dynamic gate bias technique to a class-A amplifier the average dc-rf efficiency using (8) is 35.3% which represents a moderate improvement of 7.5%. Fig. 2 illustrates the overall improvement.

SIMULATION RESULTS

To demonstrate the technique on a practical example, consider a 1 W, 2.4 mm gate-width X-band power MESFET operating at 1.88 GHz biased in class-A mode. The amplifier schematic shown in Fig. 4 utilizes the nonlinear FET model shown in Fig. 5 which is based on Maas [6] and Curtice and Ettenberg [7].

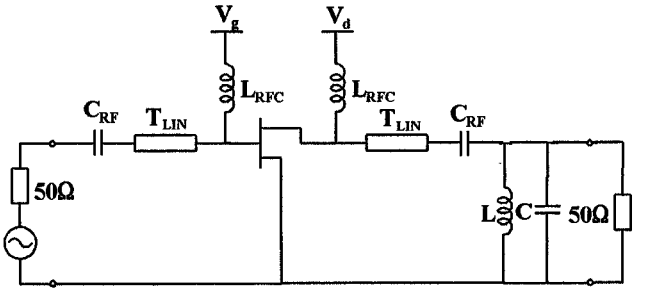

Fig. 4. Schematic of a simple single-stage power amplifier operated in class-A mode.

Fig. 6 plots the simulated output power vs. input power of the amplifier yielding 1.9 dB compression at 18 dBm input power with a gate bias voltage of -1.1 V. We let the 1.9 dB compression point correspond to the high-level 16-QAM phasors. The output powers for the mid- and low-level phasors are also indicated in Fig. 6. The corresponding dc-rf efficiencies of 45%, 27.5% and 6.3% are obtained for the fixed gate bias case yielding an average efficiency of only 26.6%.

Using the dynamic gate-biasing approach, the bias voltage for the high-level phasors remains the same but the bias voltages for the mid- and low-level phasors are adjusted to maximize dc-rf efficiency. One possible solution, as shown in Fig. 7, is to choose a constant input power to the power amplifier for all three phasor levels. Hence, we choose gate bias voltages of -1.1, -2.5 and -3 V for the high-, mid-, and low-level phasors, respectively. The resulting average efficiency is 38%. This represents a modest improvement of 11.4%. In this example, the dynamic gate bias technique causes a 28° phase shift in the low- and mid-level phasors which represents a significant amount of distortion.

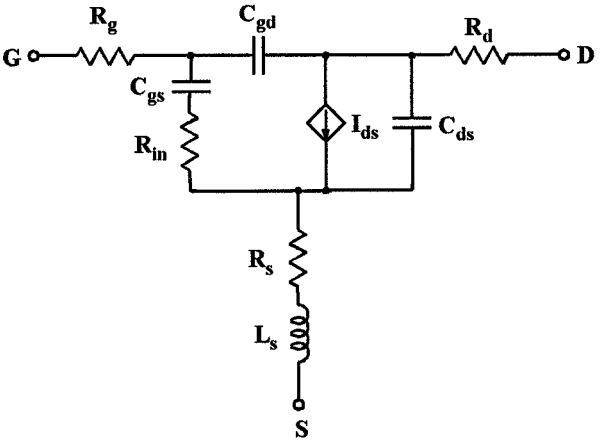

Fig. 5. Nonlinear FET model [6].

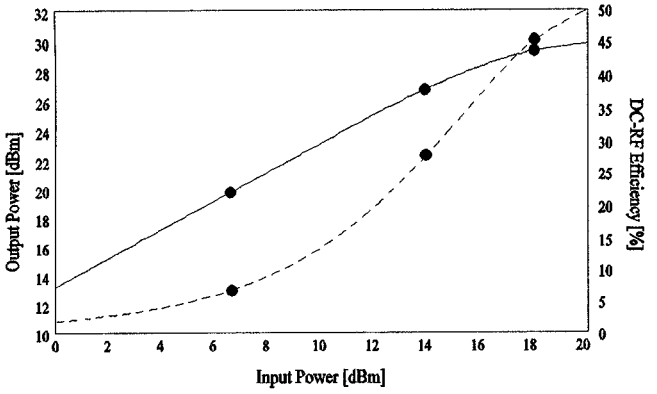

Fig. 6. Simulated output power (——) and dc-rf efficiency (– – –) vs. input power for the fixed gate bias case; (●) indicates the three phasor levels in 16-QAM.

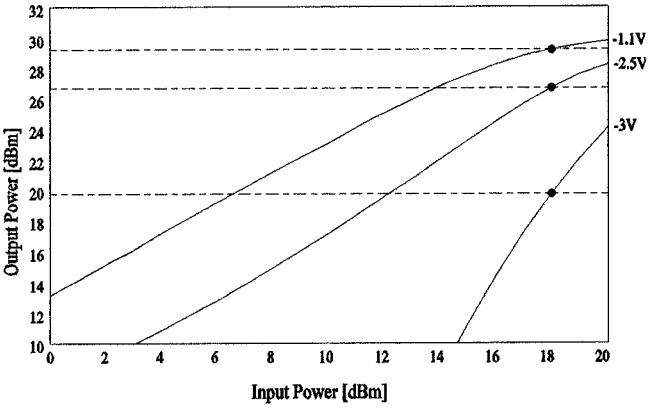

Fig. 7. Simulated output power vs. input power for the dynamic gate bias case; (●) indicates the three phasor levels in 16-QAM.

DISCUSSION

In a practical system implementation, two issues need to be addressed: nonlinear distortion of the output signal and dynamic gate bias control. One proposed system whose primary objectives are to achieve maximum efficiency in real-time while keeping nonlinear distortion to a minimum is shown in Fig. 8. The input signal is envelope detected and used to control both the high-speed bias control and the predistortion circuitry. Alternatively, if the information bits are available, the envelope detector and control circuitry can be replaced with a high-speed digital signal processor. The focus of the predistortion block is to address the nonlinear distortion inherent in the power amplifier, in addition to any nonlinear effects due to the use of dynamic biasing such as gain control and phase adjustment. Although 16-QAM was

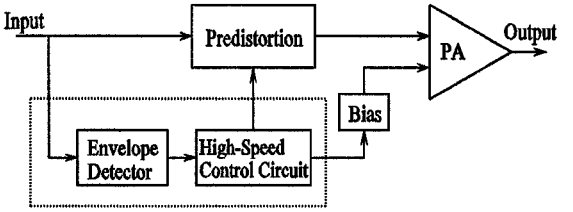

Fig. 8. Proposed system for dynamic gate bias control.

addressed in this work, we cannot neglect the benefit of increased efficiency using other popular modulation schemes currently employed. These important issues will be dealt with in future work.

REFERENCES

1. A.A.M. Saleh and D.C. Cox, "Improving the power-added efficiency of FET amplifiers operating with varying-envelope signals," *IEEE Trans. Microwave Theory Tech.*, vol. 31, 1983, pp. 51-56.

2. B.D. Geller, F.T. Assal, R.K. Gupta and P.K. Cline, "A technique for the maintenance of FET power amplifier efficiency under backoff," *IEEE MTT-S Int. Microwave Symp. Dig.*, 1989, pp. 949-952.

3. T.H. Miers and V.A. Hirsch, "A thorough investigation of dynamic bias on linear GaAs FET power amplifier performance," *IEEE MTT-S Int. Microwave Symp. Dig.*, 1992, pp. 537-540.

4. K.J. Youn, B. Kim, C.S. Lee, S.J. Maeng, J.J. Lee, K.E. Pyun and H.M. Park, "Low dissipation power and high linearity PCS power amplifier with adaptive gate bias control circuit," *Electronics Letters*, vol. 32, 1996, pp. 1533-1535.

5. *OSA90/hope*™, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1997.

6. S.A. Maas, *Nonlinear Microwave Circuits*, Artech House, Norwood, MA., 1988.

7. W.R. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 33, 1985, pp. 1383-1394.